ABSTRACT OF THE DISCLOSURE

An apparatus for circuit design verification according to an embodiment of the present invention has a verification result collector configured to collect a verification result, a data conversion and registration module configured to convert the verification result to a pre-analysis indication file, an analysis information collector configured to collect analysis information about a redundant non-active portion, an analysis information processor configured to exclude an affect of the redundant non-active portion and make an analysis indication file, an indication file storage portion configured to store the analysis indication file, and a data indication controller configured to output the analysis indication file.